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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,715	03/09/2001	Jia Li	91-C-127C1 (STMI01-00022)	1849

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EXAMINER	
MALDONADO, JULIO J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/803,715	LI, JIA
	Examiner	Art Unit
	Julio J. Maldonado	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 32-47* is/are pending in the application.

4a) Of the above claim(s) *46 and 47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 32-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/28/2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 32, 35, 38, 39, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (U.S. 5,169,792).

Katoh et al. (Fig.1A-1F) teach a method of forming isolation regions including providing a first region (logic element side) and a second region (memory element side) within a substrate (100); forming an oxidation barrier (103) made of silicon nitride on a surface of the substrate (100) over the first and second regions; forming a first patterned layer (104, 104a) exposing first isolation areas in the first region and covering substantially all of the second region and active device areas in the first region, wherein said forming of said patterned layer includes forming a photoresist layer on said

oxidation barrier (103) followed by an exposure step and a patterning step, forming said first patterned layer (104, 104a); removing portions of the oxidation barrier layer (103) exposed by the first patterned layer (104, 104a) to expose the first isolation areas; implanting a first channel-stop dopant into the first isolation areas exposed by the first patterned layer (104, 104a) and the oxidation barrier layer (103); removing the first patterned layer (104, 104a); forming a second patterned layer (104b, 104c) exposing second isolation areas in the second region and covering substantially all of the first region and active device areas in the second region; removing portions of the oxidation barrier layer (103) exposed by the second patterned layer (104b, 104c) to expose the second isolation areas; implanting a second channel-stop dopant into the second isolation areas exposed by the second patterned layer (104b, 104c) and the oxidation barrier layer (103), wherein the first isolation areas are protected by only the second patterned layer (104b, 104c) during implantation of the second channel-stop dopant into the second isolation areas.; removing the second patterned layer (104b, 104c); and growing a field oxide (106) on the first and second isolation areas where exposed by the oxidation barrier layer (103) in a single oxidation step, wherein critical dimensions for the active device areas in the first region are selected independently from critical dimensions selected for the active device areas in the second region (column 3, line 67 – column 4, line 61).

Furthermore, in another embodiment of the invention, Katoh et al. (Figs.6A-6F) teach forming isolation regions including forming n-type and p-type (601) regions within a substrate (600); forming an oxidation barrier (603) made of silicon nitride on the

surface of the substrate (600) over the n-type and the p-type (601) regions; forming a first patterned layer (604) over the n-type region and exposing isolation areas in the p-type region (601); implanting a first channel-stop dopant into the first isolation areas exposed by the first patterned layer (604) and the oxidation barrier layer (603); removing the first patterned layer (604); forming a second patterned layer (604a) exposing second isolation areas in the p-type region (601); implanting a second channel-stop dopant into the second isolation areas exposed by the second patterned layer (604a) and the oxidation barrier layer (603), wherein the first isolation areas are protected by only the second patterned layer (604a) during implantation of the second channel-stop dopant into the second isolation areas; removing the second patterned layer (604a); and growing a field oxide (606) on the first and second isolation areas where exposed by the oxidation barrier layer (603) in a single oxidation step, wherein critical dimensions for the active device areas in the p-type region are selected independently from critical dimensions selected for the active device areas in the p-type region (column 7, line 11 – column 8, line 42).

Since both embodiments of the invention ends up at the same stage prior the single oxidation step (Figs.1C and 6C), it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable forming the isolation regions disclosed in the second embodiment of the invention using the patterning process described in the first embodiment of the invention.

4. Claims 33 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (U.S. 5,169,792) as applied to claims 1, 32, 35, 38, 39 and 42 above, and further in view of Nagasawa et al. (U.S. 4,110,899).

Katoh et al. teach wherein the oxidation barrier overlies an oxide layer (column 4, lines 4 – 9), but fail to teach wherein said oxide layer is patterned together with the oxidation barrier layer using the first and second patterned layers to expose the first and second isolation areas. However, Nagasawa et al. (Figs.1-6) in a related method to form isolated areas teach forming an oxide layer (3) over a substrate (1) having a p-type region (2) and an n-type region; forming an oxidation barrier layer (4) over said oxide layer (3); and patterning the oxidation barrier layer (4), thus forming isolation areas; implanting channel stop dopants on the isolation areas, wherein said patterning comprises either patterning the oxidation barrier layer (4), or patterning the oxidation barrier layer (4) and the oxide layer (3), and wherein both patterning processes end up in the formation of the field oxide (column 3, line 44 – column 6, line 12). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Katoh et al. and Nagasawa et al. to enable the patterning step of Katoh et al. to be performed according to the teachings of Nagasawa et al. because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of performing the disclosed patterning step of Katoh et al. and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

5. Claims 34 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (U.S. 5,169,792) in view of Nagasawa et al. (U.S. 4,110,899) as applied to claims 1, 32, 33, 35, 38-40 and 42 above, and further in view of Hosaka (JP 63-271956, reference AE cited in the IDS filed on 06/28/2001).

The combination of Katoh et al. and Nagasawa et al. substantially teach all aspects of the invention but fail to disclose wherein the oxidation barrier overlies a polysilicon layer on the oxide layer which is patterned together with the oxidation barrier and the oxide layer using the first and second patterned layers to expose the first and second isolation areas. However, Hosaka (Figs.1a-1g) in a related method to form isolation areas teaches sequentially forming an oxide layer (2), a polysilicon layer (3), and a nitride oxidation barrier layer (4) over a substrate (1) for the further advantage of reduce defects within the semiconductor substrate (1) (page 8, line 19 – page 12, line 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Katoh et al. and Nagasawa et al. with the teachings of Hosaka to enable forming a polysilicon layer between the oxide layer and the nitride oxidation barrier layer of Katoh et al. and Nagasawa, since as mentioned above, this would prevent formation of defects in the semiconductor substrate.

6. Claims 36, 37 and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh et al. (U.S. 5,169,792) in view of Nagasawa et al. (U.S. 4,110,899) as applied to claims 1, 32, 33, 35 and 38-40 above, and further in view of Wolf (Silicon Processing for the VLSI Era, volume 2, reference AK cited in the IDS filed on 06/28/2001).

The combined teachings of Katoh et al. and Nagasawa et al. substantially teach all aspects of the invention but fail to disclose prior to removing the first patterned layer, etching the substrate through the first patterned layer to form recesses in the first isolation areas in the n-type region and in the p-type region. However, Wolf in page 39-40 teaches fully recessed oxide LOCOS wherein a recess is formed in the substrate before oxidation (Fig.2-26). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Katoh et al. and Nagasawa et al. with the teachings of Wolf to enable modifying the oxidation process of Katoh et al. and Nagasawa et al. by employing the fully recessed LOCOS as suggested by Wolf in the p-type and in the n-type regions of Katoh et al. and Nagasawa et al., because the isolation structure obtained by the fully recessed LOCOS not only reducing bird's beak encroachment but also resulting in a planar surface topography (last paragraph of page 40).

Response to Arguments

7. Applicant's arguments filed 07/28/2005 have been fully considered but they are not persuasive.

Applicants argue, "...No motivation exists for combining selected patterning steps from the two alternative processes as proposed in the Office Action, nor does the reference provide any reasonable expectation of success in such a selective combination...". In response to this argument, the test for obviousness is not whether the features of second embodiment may be bodily incorporated into the structure of the first embodiment; nor is it that the claimed invention must be expressly suggested in any

one or all of the embodiment of the invention of Katoh et al. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, as mentioned above, since both embodiments of the invention described in Katoh et al. ends up at the same stage prior the single oxidation step (Figs.1C and 6C), it would have been obvious to one of ordinary skill in the art at the time the invention was made to enable forming the isolation regions disclosed in the second embodiment of the invention using the patterning process described in the first embodiment of the invention.

Also, applicants argue, "...the final Office Action essentially argues that the two embodiments are interchangeable, such that elements from either embodiment may be combined with or substituted for elements in the other embodiment...This reasoning is not sufficient to establish a prima facie case of obviousness because it (a) fails to provide the requisite motivation or incentive for making the proposed combination or substitution (as opposed to a motivation to try the proposed combination or substitution) and (b) is not supported by the teachings of Katoh et al., which is silent as to interchangeability of when the oxidation barrier is etched between the two processes...". In response to this argument, one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternate the embodiments disclosed by Katoh et al. to form the above mentioned isolation regions because art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Also, applicants argue, "...nothing in Katoh et al. suggest that the extra processing steps required to form the p-type well on the logic element side, or the resulting structure, are conductive to use of a single patterned resist to both pattern the oxidation barrier and mask the channel stop dopant implant...". In response to this argument, one of ordinary skill in the art at the time the invention was made would have a reasonable expectation of success that the channel stop forming method disclosed in the embodiment of Figs.1B-1C would be useful to form the structure in Figs6B-6C because the well formation is independent ~~on~~ of channel stop formation. Note in Figs. 1B-1C, wherein the same location are masked to form the channel stops.

Furthermore, applicants argue, "...both embodiments in Katoh et al. involve the same channel stop dopant (boron) in both the logic element and memory element regions, not a first channel stop dopant in the first isolation areas and a second channel stop dopant in the second isolation areas...". In response to this argument, the claims fail to teach wherein specific dopants and wherein said first and second dopants are different. Therefore, Katoh et al. reads on the claimed invention.

Conclusion

8. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (http://portal.uspto.gov/external/portal/pair) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this group is 571-273-8300. Updates can be found at http://www.uspto.gov/web/info/2800.htm.

Julio J. Maldonado
Patent Examiner
Art Unit 2823

Julio J. Maldonado
October 11, 2005

George Fourson
Primary Examiner